HDCP Specification v1.2
Amendment for HDCP-DLI Interfaces

Revision 1.0

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Revision 1.0: Initial Release

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1. INTRODUCTION

1.1 SCOPE OF THIS DOCUMENT

This document is an amendment to the High-bandwidth Digital Content Protection (HDCP) specification for the implementation of the HDCP protocol over a DLI interface. Herein, the term HDCP-DLI refers to this interface specification and devices employing it.

1.2 HDCP PROTECTION OF THE DLI VIDEO/AUDIO TRANSPORT SYSTEM

In a DLI system, an optical link is used to transport the uncompressed video/audio data from a DLI transmitter to a DLI receiver. The data transported over the DLI link needs to be protected. This amendment specifies the requirements and implementation of the HDCP protocol used to protect the video/audio content transported over the DLI link.

1.3 DEFINITIONS

Digital Light Interface (DLI): An optical light interface that can transmit digital video, audio, and data simultaneously over a single optical light link. Link options include optical fiber, or optical wireless (free space optics).

HDCP-DLI Transmitter: An HDCP transmitter that uses the DLI interface to send protected data.

HDCP-DLI Receiver: An HDCP receiver that uses the DLI interface to receive protected data.

Forward Channel: The DLI communication channel that carries data from HDCP-DLI Transmitter to HDCP-DLI Receiver.

Backward Channel: The DLI communication channel that carries data from HDCP-DLI Receiver to HDCP-DLI Transmitter.

2. AUTHENTICATION PHASE

The HDCP-DLI authentication mechanism works in the same way as that of HDMI/DVI based HDCP devices. The following sections describe the differences of operation during the authentication phase.

2.1 HDCP RELATED COMMUNICATION CHANNELS

2.1.1 DDC data exchange channel

Instead of using an I2C bus for all HDCP authentication data exchanges, HDCP-DLI uses forward (from Transmitter to Receiver) and backward (from Receiver to Transmitter) communication channels for all HDCP related data exchange.

For this reason, there is no need for I2C specific device address 0x74 and 0x75. However, HDCP-DLI uses the same register offset addresses, as outlined in Table 2-2 and Table 2-3 in the HDCP specification, revision 1.2.

For write operations, the HDCP-DLI transmitter builds a packet with the offset address, data length and associated data. It then sends the data packet to HDCP-DLI receiver via the forward DLI communication channel. The receiver will send back an acknowledge packet to the transmitter via the backward DLI channel.

The HDCP_DLI transmitter expects to receive the acknowledge packet within 2 ms. If it fails to receive the acknowledgement packet after 3 ms, it declares a write failure and it will start the same write operation.

For read operations, the HDCP-DLI transmitter builds a packet with the offset address of the register and data length to read. It then sends the packet to HDCP-DLI receiver via the forward DLI communication channel. In response to the reading packet, the HDCP-DLI receiver builds a packet with the offset address and the associated data. It then sends the packet back to the transmitter via the backward DLI communication channel.

After sending read command packet, the HDCP_DLI transmitter expects to receive the data packet from the HDCP_DLI receiver within 2ms. If it fails to receive the expected data packet after 3 ms, it declares a read failure and it will start another read operation.

If the HDCP_DLI transmitter still fails to get the expected response after two retries of the same read or write operation (three times total), it will restart the authentication process from beginning.

The HDCP-DLI write and read operation is illustrated Figure 1.

The reading operation of EDID data structure is very similar to that in the HDCP specification with one exception. 0xA0/0xA1are not used as device addresses. However, all the data structure and offset addresses remain identical. The data packet transferred from the HDCP-DLI receiver back to the HDCP-

DLI transmitter can hold up to 128 bytes of data and shall have CRC appended for error checking. To differentiate HDCP or EDID write/read operations, HDCP-DLI uses different packet type information for EDID or HDCP related packets.

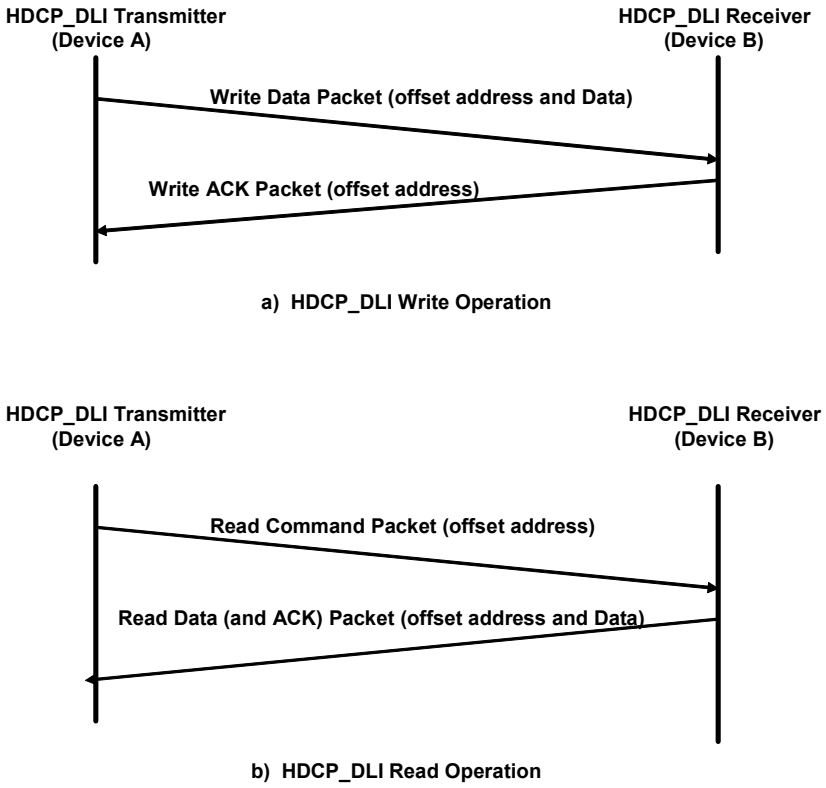

Figure 1: HDCP-DLI Write and Read Operation

2.1.2 Hot Plug Detection Indication

In the optical link, there is no physical HPD signal. Instead, the HDCP-DLI receiver sends a packet to the HDCP-DLI transmitter to show that it is ready for all EDID and HDCP operations.

The HDCP-DLI receiver can also send a packet to negate the status of the HPD status.

2.2 HDCP PROTOCOLS

2.2.1 Authentication Protocol

This amendment does not make any change to this part of the authentication protocol. Formats and values of all Keys, KSVs, and other data used for HDCP protocol are the same. Functions to calculate the intermediate values are the same.

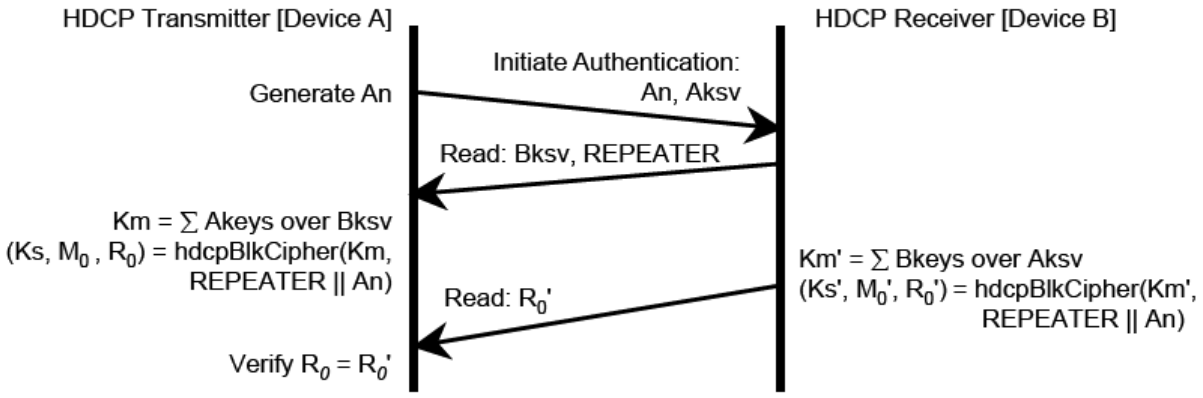

Figure 2: HDCP-DLI Authentication Process

2.2.2 Synchronization and Link Verification

In the traditional HDMI/DVI video system, both HDCP Transmitter and HDCP Receiver have counters to count the number of video frames. This frame count i or i' are used to synchronize the HDCP operation. In the DLI based system, the HDCP-DLI transmitter will have an 8 bit counter (count up to 255) to count the number of video frames. The content of this counter is transmitted to the HDCP-DLI Receiver to synchronize the HDCP operation.

After successful completion of the Authentication, the counter is reset to zero. It is incremented for every video frame (indicated by VSYNC). The counter wraps back to zero when it reaches its maximum number of 255.

If no video is present, the HDCP-DLI transmitter will still generate a frame count incremented at 60Hz frequency. This counter value is used to protect the content of audio and other data when a video signal is not present.

Besides the frame counter, the HDCP_DLI also requires that each video/audio packet contains a 20 bits packet counter field. This packet counter is reset to zero at the start of the video frame at the same time when the frame counter is incremented. It is then incremented for every video/audio packet.

Both the HDCP-DLI Transmitter and the HDCP-DLI Receiver will use this frame counter to synchronize the HDCP operation. In this way, the HDCP-DLI receiver always has the same frame counter value as the HDCP-DLI transmitter.

The link verification process is the same as that specified in HDCP V1.2. The operation is always synchronous. Ri' read and verification operations are carried out at the time of the128th Frame when the seven least significant bits of the frame counter wraps back to zero. If the read fails or Ri/Ri' comparison fails, the HDCP-DLI transmitter is required to initiate up to two more re-read and compare operations. Each Ri' read and compare operation will be 3 ms apart. If all the three read and compare operations fail, the HDCP link verification fails and the HDCP-DLI Transmitter is required to restart the HDCP authentication process.

Besides Ri verification, HDCP_DLI also requires the supporting of enhanced link verification capability. It is mandatory for the HDCP_DLI TX to read Pj' value from the HDCP_DLI RX device and compare it with its locally calculated Pj value every frame.

2.3 HDCP-DLI STATE MACHINE

This amendment does not make any change to the operation and state diagram of the HDCP transmitter and HDCP receiver.

2.4 HDCP-DLI PORT

As discussed in a previous section, all the port addresses in the HDCP-DLI are identical to that of the HDCP specification. Since there is no I2C port, 0x74 and 0x75 are not used for device access.

2.5 HDCP_DLI ENCRYPTION SIGNALING

In HDCP_DLI interface, CTL[3:0] is not transmitted over the DLI link. The HDCP_DLI protocol uses a different signaling scheme called DLIES.

In every video/audio data packets header, there is one bit called "ENC_EN" to indicate whether the current packet is encrypted or not. The encryption and decryption functions are carried out only for the packets that have ENC_EN bit set.

After successful completion of the authentication phase, the HDCP_DLI TX interface wait until the start of first video frame (first VYSNC). From that time, the HDCP_DLI TX unit will set ENC_EN bit in all video/audio frames that need be protected.

3. DATA ENCRYPTION AND HDCP CIPHER

HDCP Encryption is applied at the input of the SERDES, a device that converts parallel data to the high speed serial data for optical transmission. The decryption is applied after the output of the SERDES deserializer. Using the same methods as that in a standard HDCP implementation, HDCP-DLI encryption consists of a bitwise exclusive-OR (XOR) of the 32 bit parallel data with a 32 bit block of pseudo-random bits provided by the HDCP Cipher module. Table 1 shows the output function used by the pseudo-random number generator. It is the same as that listed in Table 4-7 of HDCP 1.3 (Amendment for Display Port).

Figure 3 shows the circuit diagram of the HDCP-DLI encryption. It is the same as that in Figure 3-1 of HDCP Specification V1.2 except that the TMDS link is replaced by DLI link. The parallel data bus width is changed from 24 bit to a standard 32 bit which is used for most SERDES application.

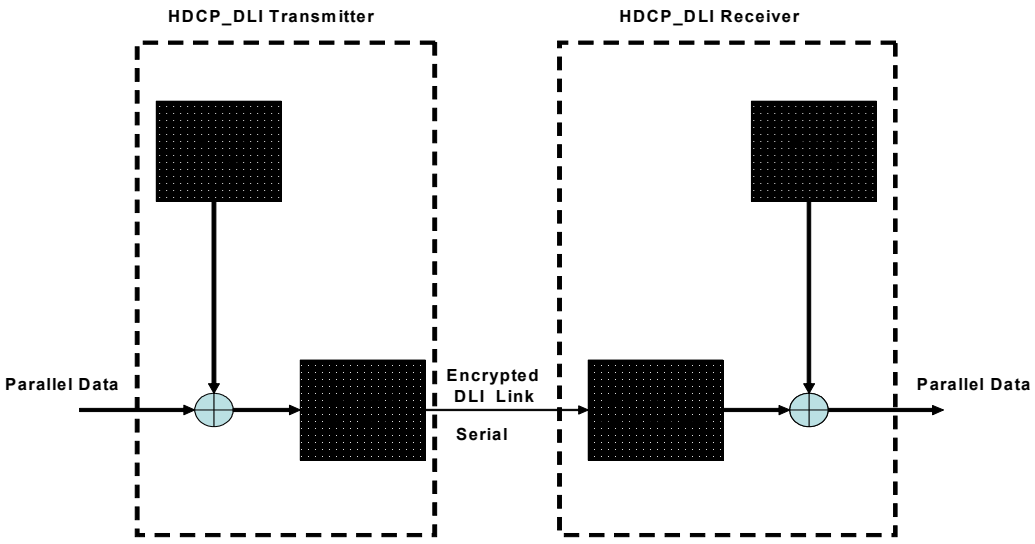

Figure 3: HDCP-DLI Encryption Diagram

Encryption and decryption operations use SERDES clock as the main clock signal.

As in the Amendment for HDCP-GVIF, the same DLI encoder/decoder is also used instead of TERC4 encoding when transmitting auxiliary data.

Input	B0	B1	B2	B3	B4	B5	B6	B7	K0	K1	K2	K3	K4	K5	K6	K7
Origin	Bz	Bz	Bz	Bz	Bz	Bz	Bz	By	Kz	Kz	Kz	Kz	Kz	Kz	Kz	Ky
Output bit																
0	17	26	22	27	21	18	2	5	3	6	0	9	4	22	5	10
1	5	20	15	24	2	25	0	16	20	18	7	23	15	5	3	25
2	22	5	14	16	25	17	20	11	7	19	2	10	22	4	13	21
3	19	3	15	11	21	16	27	1	6	14	9	8	17	18	12	24
4	19	6	17	18	22	7	9	12	25	6	5	2	10	15	21	8
5	3	7	4	8	16	6	5	17	27	14	2	4	24	19	1	12
6	8	21	27	2	11	24	12	3	17	26	4	16	27	7	22	11
7	9	5	7	4	8	13	3	15	9	10	19	11	7	6	8	23
8	26	13	23	10	11	7	15	19	13	12	18	24	15	23	7	16
9	1	0	19	11	13	16	24	18	0	5	20	25	1	24	9	27
10	26	13	9	14	10	4	1	2	14	23	27	25	17	19	1	22
11	21	15	5	3	13	25	16	27	6	21	17	15	26	11	16	7
12	20	7	18	12	17	1	16	0	11	22	20	0	26	23	17	2
13	14	23	1	12	24	6	18	9	8	4	3	14	20	26	23	15
14	19	6	21	25	23	1	10	8	19	0	18	2	13	8	24	14
15	3	0	27	23	19	8	4	7	16	21	24	25	12	27	15	18
16	6	5	14	22	24	18	2	21	3	5	8	25	7	27	2	26
17	3	4	2	6	22	14	12	26	11	14	23	17	22	13	19	4
18	25	21	19	9	10	15	13	22	1	16	14	11	12	6	10	19
19	23	11	10	20	1	12	14	4	21	1	10	20	18	26	9	13
20	11	26	20	17	8	23	0	24	20	21	9	25	12	3	15	0
21	9	17	26	4	27	0	15	6	18	12	21	27	1	16	24	20
22	22	12	2	10	7	20	25	13	13	0	3	16	22	11	26	9
23	27	24	26	8	0	9	18	23	2	0	13	5	4	8	10	3
24	5	18	27	23	17	7	8	14	23	24	0	19	1	13	25	17
25	26	11	9	24	21	15	6	25	16	21	15	27	3	26	11	1
26	19	4	20	16	22	3	14	20	4	10	14	5	9	20	22	6
27	2	12	25	13	10	1	0	10	6	17	7	8	18	2	12	5
28	12	21	2	1	18	3	13	5	23	0	22	20	12	25	24	20
29	16	5	7	4	15	10	27	2	7	8	6	3	19	9	11	19
30	26	6	23	14	11	22	17	4	4	15	26	10	14	2	13	15
31	19	25	20	8	9	24	0	8	16	18	21	1	27	5	17	27

Table 1: HDCP Cipher Output function

4. RENEW-ABILITY

This amendment does not make any change to the functions of the renew-ability of HDCP devices.

5. REFERENCE

1. High-bandwidth Digital Content Protection System, Rev 1.2, June 13, 2006, Digital Content Protection LLC.
2. High-bandwidth Digital Content Protection System, V1.3, , Amendment for Display Port, Revision 1.0, Digital Content Protection LLC
3. HDCP Specification,V1.1, , Amendment for HDCP-GVIF, Revision 1.0, Digital Content Protection LLC